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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/615,503	07/13/2000	NOBUAKI HASHIMOTO	101929.02	3462

25944 7590 12/09/2005

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/615,503	HASHIMOTO, NOBUAKI	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *10 and 11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9-16-5 has been entered.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9 and 12-20 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Marrs (5583378).

The Decision on Appeal, filed on 7-19-5, at page 9, last paragraph, states, "Thus, it would appear that Marrs, alone, teaches the invention broadly set forth in instant claim 1."

In addition, Marrs discloses the newly amendatory limitations, "individual semiconductor" because the substrates 280G are supporting materials existing as distinct entities, on which, semiconductors are fabricated.

As further noted in the Decision on Appeal, in the Brief on Appeal, filed on 5-19-4, applicant grouped claims 2-9 and 12-20 to stand or fall with claim 1. Therefore, claims 2-9 and 12-20 fall with claim 1 and are unpatentable in view of Marrs.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-4, 9 and 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Shim (5905633) and Heo (6021563).

At column 1, line 18 to column 2, line 1; and column 3, line 51 to column 5, line 46, Shim discloses the following:

A method of fabricating a semiconductor device comprising: (a) attaching a plurality of semiconductor chips 20 to a tape 60; (b) cutting the tape to obtain individual semiconductor substrates after the step (a) (see column 2, lines 12-35, and column 4, lines 26-38); and (c) providing a plurality of external terminals 50 on each of the individual semiconductor substrates, wherein the steps (a) and (b) are carried out in a reel-to-reel transport system; attaching a reinforcing member 10 to the tape in positions corresponding to each of the semiconductor chips, before the step (b); wherein the tape is cut into regions 64 each including one of the semiconductor chips in the step (b); wherein a plurality of device holes 61 are formed in the tape, and leads 11 are formed on the tape, which end portions project into the respective device holes; and wherein each of the semiconductor chips is disposed within a respective one of the device holes, and the electrodes "chip pads" of the semiconductor chips and the leads are bonded in the step (a); wherein each of the semiconductor chips is bonded to the tape in a face-up configuration in the step (a); wherein the electrodes of the semiconductor chips and leads formed on the tape are electrically connected by means of wires 30 in the step (a); attaching a heat radiating

member 64 to each of the semiconductor chips; attaching the heat radiating member before the step (b), with a reel-to-reel transport system.

A semiconductor device fabricated by the method as defined in claim 1.

A circuit board "mother board" having mounted the semiconductor device as defined in claim 18.

An electronic apparatus "BGA package" including the semiconductor device as defined in claim 18.

However, Shim does not appear to explicitly disclose providing the plurality of external terminals on each of the individual semiconductor substrates after the step (b).

Nonetheless, at column 2, lines 10-65; and column 6, lines 1-5, Heo discloses providing a plurality of external terminals "solder ball" on each of individual semiconductor substrates 11 after steps of attaching a plurality of semiconductor chips "chip" to a tape 10 and cutting the tape to obtain the individual semiconductor substrates. Furthermore, it would have been obvious to combine this disclosure of Heo with the disclosure of Shim because it would avoid damage and interference to and with the external terminals during the cutting step.

Claims 1-9 and 12-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shim (5905633) as applied to claims 1-4, 9 and 12-20 supra, and further in combination with Marrs (5583378).

At column 1, line 18 to column 2, line 1; and column 3, line 51 to column 5, line 46, Shim discloses the following:

The Decision on Appeal, filed on 7-19-5, affirmed the following rejection:

At column 1, line 18 to column 2, line 1; and column 3, line 51 to column 5, line 46, Shim discloses the following:

A method of fabricating a semiconductor device comprising: (a) attaching a plurality of semiconductor chips 20 to a tape 60; (b) cutting the tape to obtain substrates after the step (a) (see column 2, lines 12-35, and column 4, lines 26-38); and (c) providing a plurality of external terminals 50 on each of the substrates, wherein the steps (a) and (b) are carried out in a reel-to-reel transport system; attaching a reinforcing member 10 to the tape in positions corresponding to each of the semiconductor chips, before the step (b); wherein the tape is cut into regions 64 each including one of the semiconductor chips in the step (b); wherein a plurality of device holes 61 are formed in the tape, and leads 11 are formed on the tape, which end portions project into the respective device holes; and wherein each of the semiconductor chips is disposed within a respective one of the device holes,

and the electrodes "chip pads" of the semiconductor chips and the leads are bonded in the step (a); wherein each of the semiconductor chips is bonded to the tape in a face-up configuration in the step (a); wherein the electrodes of the semiconductor chips and leads formed on the tape are electrically connected by means of wires 30 in the step (a); attaching a heat radiating member 64 to each of the semiconductor chips; attaching the heat radiating member before the step (b), with a reel-to-reel transport system.

A semiconductor device fabricated by the method as defined in claim 1.

A circuit board "mother board" having mounted the semiconductor device as defined in claim 18.

An electronic apparatus "BGA package" including the semiconductor device as defined in claim 18.

Although Shim does not appear to explicitly disclose providing the plurality of external terminals on each of the substrates after the step (b), at column 9, lines 33-41; column 10, lines 11-49; and column 15, lines 33-45, Marrs discloses providing a plurality of external terminals 218J on each of substrates 280G after steps of attaching a plurality of semiconductor chips 202H to a tape 299E and cutting the tape to obtain the substrate. Furthermore, it would have been obvious to combine the disclosure of Marrs

and Shim because, as disclosed by Marrs, particularly at column 10, lines 29-32, it would facilitate cost effective and efficient mass production.

Also, Shim does not appear to explicitly disclose wherein the tape is cut into regions each including two or more of the semiconductor chips in the step (b); and cutting each of the substrates into regions, each including one of the semiconductor chips, after the step (c).

Nevertheless, as cited, Marrs discloses wherein a tape is cut into regions 280G each including two or more semiconductor chips, and cutting each of the substrates into regions 270F, each including one of the semiconductor chips, after the step of providing the plurality of external terminals on each of the substrates. In addition, it would have been obvious to combine the disclosure of Marrs with the disclosure of Shim because it would facilitate cost effective and efficient mass production.

In addition, both Shim and Marrs disclose the newly amendatory limitations not specifically addressed in the Decision on Appeal, "individual semiconductor" because the substrates of both Shim and Marrs are supporting materials existing as distinct entities, on which, semiconductors are fabricated.

Applicant's remarks filed 9-16-5 have been fully considered and are adequately addressed by the rejections supra.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions relevant to the examination of the instant invention.

For information on the status of this application applicant should check PAIR: Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
6-Dec-05